Amendments to the Claims

1. (Original) A metal-insulator-metal capacitor process, comprising:

forming a first dielectric layer on a substrate;

forming a first metal layer in the first dielectric layer;

forming a stop layer on the first dielectric layer;

forming a second dielectric layer on the stop layer;

forming a first patterned mask layer on the second dielectric layer;

performing an etching process, using the first patterned mask layer as an etching mask, so that a first opening and a second opening are formed in the second dielectric layer, thereby exposing portions of the stop layer above a first region and a second region of the first metal layer, respectively;

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forming a second patterned mask layer on the second dielectric layer and a part of the stop layer;

performing a further etching process, using the second patterned mask layer as a further etching mask, to etch the stop layer below the second opening and to partially etch a third opening adjacent the second opening in the second dielectric layer without exposing the stop layer thereunder; and

forming a second metal layer over the substrate so as to fill the first, second and third openings;

wherein a metal-insulator-metal (MIM) capacitor is formed by the first region of the first metal layer, the stop layer and the filled first opening, and the filled second opening forms a via between the first and second metal layers, and the first and second metal layers include copper.

2. (Original) The process according to claim 1, wherein the first dielectric layer includes a silicon oxide layer.

3. (Original) The process according to claim 1, wherein the stop layer includes a silicon nitride layer.

4. (Original) The process according to claim 1, wherein the second dielectric layer includes a silicon oxide layer.

5. (Original) The process according to claim 1, wherein the second metal layer is polished by chemical-mechanical polishing.

6. (Original) The process according to claim 1, wherein said forming the first metal layer includes polishing by chemical-mechanical polishing.

7. (Original) The process according to claim 1, wherein the first and second dielectric layers are thicker than the stop layer.

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8. (Original) A metal-insulator-metal capacitor process, comprising:

forming a first dielectric layer on a substrate;

forming a first patterned masking layer over the substrate such that a portion of the first dielectric layer is exposed;

removing only a depth-wise portion the exposed portion of the first dielectric layer such that the substrate is not exposed;

filling the removed portions of the first dielectric layer with a copper or copper alloy thereby forming a first metal layer;

forming a stop layer on the first dielectric layer and the first metal layer;

forming a second dielectric layer on the stop layer;

forming a second patterned masking layer over the substrate such that a portion of the second dielectric layer is exposed;

removing the exposed portion of the second dielectric layer, so that a first opening and a second opening are formed in the second dielectric layer, thereby exposing portions of the stop layer above a first region and a second region of the first metal layer, respectively;

forming a third patterned masking layer over the substrate such that a further portion of the second dielectric layer and a portion of the stop layer are exposed;

removing the exposed portions of the second dielectric layer and the stop layer, thereby exposing a portion of the second region of the first metal layer;

filling the first and the second openings with a copper or copper alloy thereby forming a second metal layer;

wherein a metal-insulator-metal (MIM) capacitor is formed by the first region of the first metal layer, the stop layer and the filled first opening, and the filled second opening forms a via between the first and second metal layers.

9. (Original) The process according to claim 8, wherein the first dielectric layer includes a silicon oxide layer.

10. (Original) The process according to claim 8, wherein the stop layer includes a silicon nitride layer.

11. (Original) The process according to claim 8, wherein the second dielectric layer includes a silicon oxide layer.

12. (Original) The process according to claim 8, wherein the second metal layer is polished by chemical-mechanical polishing.

13. (Original) The process according to claim 8, wherein said forming the first metal layer includes polishing by chemical-mechanical polishing.

14. (Original) The process according to claim 8, wherein the first and second dielectric layers are thicker than the stop layer.

15. (Original) A metal-insulator-metal (MIM) capacitor process, comprising:

forming a first metal layer on a substrate, wherein a portion of the first metal layer is utilized as the lower plate of the MIM capacitor;

forming an etch stop layer on the substrate and the first metal layer, wherein a portion of an etch stop layer is utilized as the insulator for the MIM capacitor; and

forming a second metal layer on the substrate and portion of an etch stop layer, wherein a portion of the second metal layer is utilized as the upper plate of the MIM capacitor;

wherein the first and the second metal layers include copper or a copper alloy.

16. (Original) The process according to claim 15, wherein the stop layer includes a silicon nitride layer.

17. (Original) The process according to claim 15, wherein the second metal layer is polished by chemical-mechanical polishing.

18. (Original) The process according to claim 15, wherein the first metal layer is polishing by chemical-mechanical polishing.